Amendments to the Specification

Please replace the abstract with the following amended abstract:

A UART sets a predetermined threshold remaining data amount *n*, which defines an interrupt position, in a transmission trigger detector before data transmission is completed, checks if a trigger, which indicates the value of a read pointer RP or a count value N has reached a position indicated by the setting, has ~~occurs~~ occurred and, if the trigger ~~occurs~~ has occurred, causes a trigger detector to output a interrupt output control signal to an internal interrupt circuit to perform internal interrupt processing. Upon detecting this trigger, the internal interrupt circuit outputs an internal interrupt signal. When all data has not yet been transmitted from a transmission FIFO circuit, a CPU of a host controls the amount of data to be transferred to the transmission FIFO circuit, considering the threshold *n*, to prevent data in that circuit from being overwritten.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Canceled):

Claim 2 (Currently Amended): The communication terminal in accordance with claim [[1]] 18, wherein, [[even]] when the data has been ~~transmitted~~ outputted from said transmission buffer circuit, said transmission buffer control circuit assigns priority to an operation of said transmission buffer monitoring circuit ~~that indicates~~ indicating that the data is being transmitted to the host and inhibits said interrupt circuit from generating the interrupt signal ~~from being sent to said interrupt circuit~~.

Claim 3 (Currently Amended): The communication terminal in accordance with claim [[1]] 18, wherein said transmission buffer control circuit includes said transmission buffer monitoring circuit.

Claim 4 (Currently Amended): The communication terminal in accordance with claim 2, wherein said transmission buffer control circuit includes said transmission buffer monitoring circuit.

Claim 5 (Currently Amended): The communication terminal in accordance with claim [[1]] 18, wherein said communication terminal is included in a radio device that performs radio transmission.

Claim 6 (Currently Amended): The communication terminal in accordance with claim 2, wherein said communication terminal is included in a radio device that performs radio transmission.

Claim 7 (Currently Amended): The communication terminal in accordance with claim 3, wherein said communication terminal is included in a radio device that performs radio transmission.

Claim 8 (Currently Amended): The communication terminal in accordance with claim 4, wherein said communication terminal is included in a radio device that performs radio transmission.

Claim 9 (Currently Amended): The communication terminal in accordance with claim 5, wherein said radio device conforms to a Bluetooth communication standard.

Claim 10 (Currently Amended): The communication terminal in accordance with claim

6, wherein said radio device conforms to a Bluetooth communication standard.

Claim 11 (Currently Amended): The communication terminal in accordance with claim 7, wherein said radio device conforms to a Bluetooth communication standard.

Claim 12 (Currently Amended): The communication terminal in accordance with claim 8, wherein said radio device conforms to a Bluetooth communication standard.

Claims 13-17 (Canceled)

Claim 18 (New): A communication terminal for transmitting and receiving data to and from a host, comprising:

a transmission buffer circuit that maintains a continuous transmission of the data, and that stores therein the data according to a first write pointer designating an address location which the data is to temporarily be written into, and that reads out the data stored according to a first read pointer designating an address location where the data is stored;

a reception buffer circuit that stores therein the data received by the host according to a second write pointer designating an address location which the data is to temporarily be written into, and that reads out the data stored according to a second read pointer designating an address location where the data is stored;

a transmission buffer control circuit that generates a first write count signal according to the first write pointer and a first read count signal according to the first read pointer, and that controls write-in and read-out of the data in said transmission buffer circuit;

a reception control circuit that generates a second write count signal according to the second write pointer and a second read count signal according to the second read pointer, and that controls write-in and read-out of the data in said reception buffer circuit;

a transmission buffer monitoring circuit that monitors whether or not a first condition is satisfied under which a difference between the first write count signal and the first read count signal exceeds a first predetermined value, and that generates a first trigger signal when the first condition is not satisfied;

a reception buffer monitoring circuit that monitors whether or not a second condition is satisfied under which a difference between the second write count signal and the second read count signal exceeds a second predetermined value, and that generates a second trigger signal when the second condition is not satisfied; and

an interrupt circuit, operative responsive to at least one of the first and second trigger signals, that generates an interrupt signal,

said interrupt circuit providing the host with the interrupt signal to cause the data to be transmitted and received to and from the host.

Claim 19 (New): A method of transmitting data between a communication terminal and a host in response to an interrupt signal supplied to the host, comprising;

preparing a communication terminal including a transmission buffer circuit and a reception buffer circuit for preventing data from being lost in transmission and reception, respectively;

providing the transmission buffer circuit with a first write pointer designating an address location which the data is to temporarily be written into and a first read pointer designating an address location where the data is temporarily stored, and setting a first storable data amount representative of a difference of the first write pointer from a storage capacity of the transmission buffer circuit as a timing position at which the interrupt signal is to be generated;

providing the reception buffer circuit with a second write pointer designating an address location which the data is to temporarily be written into and a second read pointer designating an address location where the data is temporarily stored, and setting a second storable data amount representative of a difference of the second write pointer from a storage capacity of the reception buffer circuit as a timing position at which the interrupt signal is to be generated;

transmitting the data between the host and the communication terminal;

generating a first write count signal and a first read count signal in response to the first write pointer and the first read pointer, respectively, and determining whether or not the first storable data amount is coincident with the first read pointer to monitor the

transmission buffer circuit;

generating a second write count signal and a second read count signal in response to the second write pointer and the second read pointer, respectively, and determining whether or not the second storable data amount is coincident with the second read pointer to monitor the reception buffer circuit;

generating a first trigger signal in response to the first storable data amount being coincident with the first read pointer, to control the transmission buffer circuit;

generating a second trigger signal in response to the second storable data amount being coincident with the second read pointer, to control the reception buffer circuit;

responding to at least one of the first and second trigger signals and generating the interrupt signal to be supplied to the host; and

determining whether or not the data is to be transmitted in response to the interrupt signal generated,

wherein if the data is to be kept being transmitted, returning to said preparing, and wherein if transfer of the data is to be terminated, the transmission of the data is terminated,

whereby transmission and reception of the data are performed simultaneously and separately from each other.

Claim 20 (New): The method in accordance with claim 19, wherein in said generating a

first trigger signal, when the data has been outputted from the transmission buffer circuit and the data is being transmitted, priority is assigned to transmission of the data and generation of the interrupt signal is inhibited in said responding to at least one of the first and second trigger signals.

Claim 21 (New): The method in accordance with claim 19, wherein the host checks whether or not the interrupt signal is received, and, if the interrupt signal is received, the host performs other task processing while said transmitting the data, said generating a first write count signal and a first read count signal, said generating a second write count signal and a second read count signal, said generating a first trigger signal, said generating a second trigger signal, and said responding to at least one of the first and second trigger signals are executed.

Claim 22 (New): The method in accordance with claim 20, wherein the host checks whether or not the interrupt signal is received, and, if the interrupt signal is received, the host performs other task processing while said transmitting the data, said generating a first write count signal and a first read count signal, said generating a second write count signal and a second read count signal, said generating a first trigger signal, said generating a second trigger signal, and said responding to at least one of the first and second trigger signals are executed.

Claim 23 (New): A communication terminal comprising:

an internal data bus that transfers data;

a transmit data memory that stores data transferred over said internal data bus according to a first write pointer designating an address location which the data is to temporarily be written into, and that reads out the data stored according to a first read pointer designating an address location where the data is stored;

a transmission controller that generates a first write count signal according to the first write pointer and a first read count signal according to the first read pointer, that generates a first interrupt signal according to the first write count signal and the first read count signal, and that controls a flow of the data over said internal data bus to said transmit data memory based on a processing rate of said transmit data memory;

a transmit shift register that stores the data read out from said transmit data memory and that outputs the data;

a receive shift register that stores data input from an external unit and that outputs the data stored;

a receive data memory that stores the data output from said receive shift register according to a second write pointer designating an address location which the data is to temporarily be written into, and that reads out the data stored according to a second read pointer designating an address where the data is stored; and

a reception controller that generates a second write count signal according to the second write pointer and a second read count signal according to the second read

pointer, that generates a second interrupt signal according to the second write count signal and the second read count signal, and that controls a flow of the data over said internal data bus to said receive data memory based on a processing rate of said receive data memory.